WHAT IS CLAIMED IS:

1. A shift register including of a plurality of unit circuits each having:

a shifter comprising a NAND circuit to receive an input pulse as one input thereof; and

a holder having a PMOS transistor and an NMOS transistor, which are connected in series between a power supply and a clock input end fed with a clock pulse and of which gates and drains are mutually connected in common respectively, wherein the input end of said holder is connected to the output end of said NAND circuit, and the output potential thereof is fed as another input to said NAND circuit.

2. The shift register according to claim 1, wherein said unit circuits are cascade-connected to form a plurality of stages, and the odd-stage unit circuits and the even-stage unit circuits operate in synchronism respectively with clock pulses having a 1/4 phase difference from each other.

3. The shift register according to claim 1, further having a PMOS transistor connected in parallel with the NMOS transistor in said holder and receiving, as a gate input thereto, a pulse opposite in phase to the input pulse fed to said holder.

4. The shift register according to claim 3, further having an inverter circuit, which inverts the phase of the input pulse fed to said holder and then feeds the phase-inverted pulse to the gate of said PMOS transistor.

5. The shift register according to claim 1, further having a waveform shaping shift circuit, which shapes the waveform of the input pulse in synchronism with the clock pulse having a 1/4 phase difference from the clock pulse fed to said holder, and then feeds the waveform-shaped pulse to said shifter.

6. The shift register according to claim 5, further having an inverter circuit for inverting the phase of said input pulse and feeding the phase-inverted pulse to said waveform shaping shift circuit.

7. A display device having:

a plurality of pixels arrayed two-dimensionally; and

a scanner for selecting each of said plural pixels column by column or row by row;

wherein said scanner is composed of a shift register comprising a plurality of unit circuits cascade-connected to form a plurality of stages, each unit circuit having:

a shifter comprising a NAND circuit to receive an input pulse as one input thereof; and a holder having a PMOS transistor and an NMOS transistor, which are connected in series between a power supply and a clock input end fed with a clock pulse and of which gates and drains are mutually connected in common respectively, wherein the input end of said holder is connected to the output end of said NAND circuit, and the output potential thereof is fed as another input to said NAND circuit; and the odd-stage unit circuits and the even-stage unit circuits operate in synchronism respectively with clock pulses having a 1/4 phase difference from each other.

8. The display device according to claim 7, further having a PMOS transistor connected in parallel with the NMOS transistor in said holder and receiving, as a gate input thereto, a pulse opposite in phase to the input pulse fed to said holder.

9. The display device according to claim 8, further having an inverter circuit, which inverts the phase of the input pulse fed to said holder and then feeds the phase-inverted pulse to the gate of said PMOS transistor.

10. The display device according to claim 7, further having a waveform shaping shift circuit, which

shapes the waveform of the input pulse in synchronism with the clock pulse having a 1/4 phase difference from the clock pulse fed to said holder, and then feeds the waveform-shaped pulse to said shifter.

11. The display device according to claim 10, further having an inverter circuit for inverting the phase of said input pulse and feeding the phase-inverted pulse to said waveform shaping shift circuit.

12. The display device according to claim 7, wherein said plurality of pixel display elements are liquid crystal cells.